In The Claims

Claims 17, 18, 29-39, 49, 50, and 52-65 are pending in the application with claim 50 amended herein and claim 51 cancelled herein.

Claims 1-16 (cancelled).

17. (previously presented) An electronic apparatus fabrication method comprising:

forming a mixture of a powder comprising aluminum, a powder comprising silicon, and a powder comprising carbon;

mechanically activating the mixture and allowing the mixture to react by spontaneous ignition by exposing the mixture to oxygen gas and to an inert gas excluding nitrogen;

forming the reacted mixture into an insulative plate comprising an aluminum-based glass; and

forming a layer comprising a semiconductive material over the plate.

18. (original) The method of claim 17 wherein allowing the mixture to react comprises exposing the mixture to air.

Claims 19-28 (cancelled).

29. (previously presented) A silicon-on-insulator integrated circuit fabrication method comprising:

forming a mixture of a powder comprising aluminum, a powder comprising silicon, and a powder comprising carbon;

mechanically activating the mixture and allowing the mixture to react by spontaneous ignition;

forming the reacted mixture into an insulative glass substrate comprising aluminum oxycarbide;

removing a layer of silicon from a monocrystalline silicon wafer;

bonding the silicon layer on and in contact with the glass substrate; and

forming a semiconductor device comprising at least a part of the silicon layer.

30. (original) The method of claim 29 wherein the glass substrate further comprises aluminum carbide, silicon carbide, and α-alumina.

31. (original) The method of claim 29 wherein allowing the mixture to react comprises exposing the mixture to air.

32. (original) The method of claim 29 wherein allowing the mixture to react comprises exposing the mixture to oxygen gas and an inert gas that does not comprise nitrogen.

33. (original) The method of claim 29 wherein the glass substrate exhibits a CTE sufficiently close to a CTE of the silicon layer such that a strain of less than 1% would exist between a 1000 Å thickness of the silicon layer and the glass substrate.

34. (original) The method of claim 33 wherein the silicon layer has a thickness of about 1000 Å or less.

35. (original) The method of claim 33 wherein the strain would be less than 0.6%.

36. (original) The method of claim 29 wherein removing the layer of silicon comprises implanting ions into the wafer.

37. (original) The method of claim 29 wherein bonding the silicon layer comprises heating to at least 400 °C.

38. (original) The method of claim 29 wherein bonding the silicon layer comprises laser assisted annealing.

39. (original) The method of claim 29 further comprising chemically-mechanically polishing the silicon layer after bonding to the glass substrate.

Claims 40-48 (canceled).

49. (previously presented) The method of claim 17 wherein the aluminum-based glass comprises aluminum oxycarbide.

50. (currently amended) An electronic apparatus fabrication method comprising:

forming a mixture of a powder comprising aluminum, a powder comprising silicon, and a powder comprising carbon;

mechanically activating the mixture and allowing the mixture to react by spontaneous ignition by exposing the mixture to oxygen gas and an inert gas that does not comprise nitrogen;

forming the reacted mixture into an insulative plate comprising an aluminum-based glass; and

forming a layer comprising a semiconductive material over the plate, a composition of the mixture being selected so the plate exhibits a CTE sufficiently close to a CTE of the semiconductive layer that a strain of less than 1% would exist between a 1000 Å thickness of the semiconductive layer and the plate.

51. (cancelled).

52. (previously presented) The method of claim 50 wherein the semiconductive layer has a thickness of about 1000 Å or less.

53. (previously presented) The method of claim 50 wherein the strain would be less than 0.6%.

54. (previously presented) An electronic apparatus fabrication method comprising:

forming an insulative glass substrate with components comprising aluminum oxycarbide, aluminum carbide, silicon carbide, and α-alumina; and

forming a layer comprising a semiconductive material over the substrate, a content of the components in the glass substrate being selected prior to forming the glass substrate so it exhibits a CTE sufficiently close to a CTE of the semiconductive layer that a strain of less than 1% would exist between a 1000 Å thickness of the semiconductive layer and the glass substrate.

55. (previously presented) The method of claim 54 further comprising forming a semiconductor device comprising at least a part of the semiconductive material layer.

56. (previously presented) The method of claim 54 wherein the semiconductive material layer is formed on and in contact with the insulative substrate.

57. (previously presented) The method of claim 54 wherein the semiconductive material layer has a thickness of about 1000 Å or less.

58. (previously presented) The method of claim 54 wherein the strain would be less than 0.6%.

59. (previously presented) The method of claim 54 wherein forming the semiconductive material layer comprises:

removing a layer of silicon from a monocrystalline silicon wafer; and

bonding the silicon layer to the insulative substrate.

60. (previously presented) The method of claim 59 wherein removing the layer of silicon comprises implanting ions into the wafer.

61. (previously presented) The method of claim 59 wherein bonding the silicon layer comprises heating to at least 400 °C.

62. (previously presented) The method of claim 59 wherein bonding the silicon layer comprises laser assisted annealing.

63. (previously presented) The method of claim 59 wherein bonding the silicon layer comprises activating a surface of at least the silicon wafer by exposure to a plasma.

64. (previously presented) The method of claim 54 further comprising chemically-mechanically polishing the semiconductive material layer.

65. (previously presented) The method of claim 54 wherein the insulative substrate further comprises silicon.